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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,936	01/16/2004	Rajat Chaudhry	AUS920030974US1	8220

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Gregory W. Carr
670 Founders Square
900 Jackson Street
Dallas, TX 75202

EXAMINER	
DAY, HERNG DER	

ART UNIT	PAPER NUMBER
2128	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/759,936	CHAUDHRY ET AL.	
	Examiner	Art Unit	
	Herng-der Day	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is in response to Applicants' Response ("Response") to Office Action dated December 5, 2006, filed March 5, 2007.

1-1. Claims 1, 9, and 14-17 have been amended. Claims 1-24 are pending.

1-2. Claims 1-24 have been examined and rejected.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-24 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

3-1. Each of the amended independent claims 1, 9, and 17 recites the added limitation, "storing, for subsequent use, an operational model based on the generated power consumption data" or its equivalent in the claim. However, "storing, for subsequent use, an operational model" does not appear to have support in the original disclosure. In other words, no evidence in the original disclosure can be found to support the added limitation.

3-2. Claims not specifically rejected above are rejected as being dependent on a rejected claim.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Radjassamy, U.S. Patent Application Publication No. 2004/0186703 A1 Published September 23, 2004, and filed March 20, 2003, in view of Lim et al., U.S. Patent 5,481,209 issued January 2, 1996.

5-1. Regarding claim 1, Radjassamy discloses a method for approximating power consumption of a circuit with plurality of local clock buffers (LCBs), comprising:

inputting a Hardware Descriptive Language (HDL) simulator data of the circuit (The HDL language environment provides a design, simulation, and synthesis platform, paragraph [0015]);

inputting net capacitance data of the circuit (as shown in FIG. 4, capacitance are associated with various power consumption components as capacitors);

inputting energy model data (power consumption equation P_{EST}, for power consumption component models shown in FIG. 5A-5F); and

generating power consumption data from the HDL simulator data, the capacitance data, and the energy model data (the power consumption of the entire sub-block may be estimated, paragraph [0086]).

storing, for subsequent use, an operational model based on the generated power consumption data (Schematic editors produce various data and file types, such as model files 208, paragraph [0017]).

Radjassamy fails to expressly disclose wherein the energy model data further comprises extrapolating energy data by increasing or decreasing the number of active LCBs.

Lim et al. disclose an apparatus and method for improved clock distribution and control in an integrated circuit having the ability to selectively inhibit clock signals at the local buffer 46. Using inhibit 52 to inhibit the clock at selected locations of the integrated circuit 10 allows for reduction of power dissipation (column 4, lines 62-67). Other features include locally buffered clock signals and multiple clock enables (column 3, lines 33-35).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Radjassamy to incorporate the teachings of Lim et al. to obtain the invention as specified in claim 1 because inhibiting locally buffered clock signals at selected locations results in reduced power dissipation as suggested by Lim et al.

5-2. Regarding claim 2, Radjassamy further discloses wherein each LCB of the plurality of LCBs is at least configured to consume the same amount of power (for example, I_i represents the current of clock type i, paragraph [0044]; same current for same clock type).

5-3. Regarding claim 3, Radjassamy further discloses wherein the energy model data further comprises extrapolating energy data by increasing or decreasing numbers of active input signals to the circuit (for example, activity factors, paragraph [0067]).

5-4. Regarding claim 4, Radjassamy further discloses wherein the method further comprises inputting template data, wherein the template data is at least configured to contain relative power consumption data for each LCB of the plurality of LCBs (as shown in FIG. 4 and FIG. 5A-5F, each of the various power consumption components may have its own clock input).

5-5. Regarding claim 5, Radjassamy further discloses wherein the relative power consumption data of each LCB of the plurality of LCBs are at least configured to be the same or different (for example, I_i represents the current of clock type i, paragraph [0044]; same current for same clock type).

5-6. Regarding claim 6, Radjassamy further discloses wherein each LCB of the plurality of LCBs is at least configured to consume the same amount of power (for example, I_i represents the current of clock type i, paragraph [0044]; same current for same clock type).

5-7. Regarding claim 7, Radjassamy further discloses wherein the energy model data further comprises extrapolating energy data by increasing or decreasing numbers of active input signals to the circuit (for example, activity factors, paragraph [0067]).

5-8. Regarding claim 8, Radjassamy further discloses wherein the generating power consumption data is at least configured to utilize the template data (the power consumption of the entire sub-block may be estimated by aggregating the power consumption estimates of its constituent power consuming components, paragraph [0086]).

5-9. Regarding claims 9-16, these apparatus claims include equivalent method limitations as in claims 1-8 and are unpatentable using the same analysis of claims 1-8.

5-10. Regarding claims 17-24, these computer program product claims include equivalent method limitations as in claims 1-8 and are unpatentable using the same analysis of claims 1-8.

Applicants' Arguments

6. Applicants argue the following:

(1) "Applicants have amended Claims 14-16 in this Response to recite, in relevant part, "The apparatus"" (Page 10, paragraph 5 through page 11, paragraph 1, Response).

(2) "Nevertheless, Applicants have amended Claims 1, 9, and 17 to recite, in relevant part "storing, for subsequent use, an operational model based on the generated power consumption data." Applicants respectfully submit that these amendments thus overcome the rejections under 35 U.S.C. §101, as described above." (Page 11, paragraph 3, Response).

(3) "the Examiner cannot show anywhere in Lim where Lim even hints at "reduced estimation of power dissipation." Instead, Lim teaches using LCBs to reduce actual power dissipation, not an estimated power dissipation". (Page 13, paragraph 2, Response).

(4) "Lim expressly teaches, "Inhibiting the clock at selected locations of the integrated circuit allows for reduction of power dissipation, and specific logical operations involving only part of the integrated circuit chip logic." Lim, col. 3, lines 19-22. Nowhere does Lim come anywhere close to teaching, "extrapolating energy data by increasing or decreasing the number of active LCBs," as recited in the Claims" (Page 13, paragraph 2, Response).

(5) "Therefore, even if Lim did teach this element, which ii does not, Radjassamy clearly rejects it in favor of another approach. For at least this reason, there is no motivation to combine Radjassamy with Lim, and therefore the Examiner's purported prima facie case must fail." (Page 14, paragraph 1, Response).

(6) "Furthermore, neither does Lim teach, disclose, or suggest, "storing, for subsequent use, an operational model based on the generated power consumption data," as recited in amended Claims 1, 9, and 17." (Page 14, paragraph 2, Response).

Response to Arguments

7. Applicants' arguments have been fully considered.

7-1. Applicants' argument (1) is persuasive. The rejections of claims 14-16 under 35 U.S.C. 112, second paragraph, in Office Action dated December 5, 2006, have been withdrawn.

7-2. Applicants' arguments (2) and (6) are not persuasive. These amendments may overcome the rejections under 35 U.S.C. §101. However, these amendments do not appear to have support in the original disclosure.

7-3. Applicants' arguments (3) and (5) are not persuasive. In response to Applicants' argument against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Applicants argue, "Lim teaches using LCBs to reduce actual power dissipation, not an estimated power dissipation". Nevertheless, Radjassamy discloses a method for estimating power consumption of an integrated circuit. Knowing Lim's teaching that using

LCBs may reduce actual power dissipation, it would have been obvious to one of ordinary skill in the art to incorporate Lim's teachings in estimating power consumption of an integrated circuit.

7-4. Applicants' argument (4) is not persuasive. As Applicants argued, "Lim expressly teaches, "Inhibiting the clock at selected locations of the integrated circuit allows for reduction of power dissipation"". Applicants also argued in argument (3), "Lim teaches using LCBs to reduce actual power dissipation, not an estimated power dissipation". In other words, Lim discloses the power dissipation depends on number of inhibited LCBs, which anticipates the claimed limitation, "extrapolating energy data by increasing or decreasing the number of active LCBs".

Conclusion

8. Applicants' amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicants are reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Herng-der Day whose telephone number is (571) 272-3777. The Examiner can normally be reached on 9:00 - 17:30.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: (571) 272-2100.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kamini S. Shah can be reached on (571) 272-2279. The fax phone numbers for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Herng-der Day H.D.
May 10, 2007

KAMINI SHAH
SUPERVISORY PATENT EXAMINER